Rule 1.126 SUB B' 7. A detector for detecting timing in a data flow with a bit-time, and with a coding that provides at a beginning of the bit-time no transition, or a transition of a first type, or a transition of a second type, and provides in a middle of the bit-time no transition, or the transition of the first type, the detector comprising:

a first circuit for generating four local timing signals each having a period substantially equal to the bit-time, the four local timing signals being out of phase with one another by 1/4 period; and

a second circuit for sampling the four local timing signals upon each transition of the first type in the data flow, and for determining based upon sampling whether two of the four local timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow, and for controlling said first circuit to delay or advance the four local timing signals based upon the pair of reference signals.

8. A detector according to Claim 7, wherein the coding comprises a coded mark inversion coding.

9. A detector according to Claim 7, wherein said second circuit comprises:

a sampling circuit; and

a decoding circuit connected to said sampling circuit for decoding the sampled four local timing signals, and connected to said first circuit for control thereof.

10 ~~9~~. A detector according to Claim ~~8~~ 9, wherein said sampling circuit comprises four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow; and wherein said decoding circuit comprises a logic circuit connected to respective outputs of said four bistable elements for determining whether the pair of reference signals are advanced or delayed relative to the timing of the data flow.

12 cont

11 ~~10~~. A detector according to Claim ~~9~~ 10, wherein each one of said bistable elements comprises a D-type flip-flop; and wherein said logic circuit comprises a pair of AND gates connected to the outputs of said four bistable elements, a NOR gate connected to respective outputs of said pair of AND gates, and an INVERTER connected to an output of said NOR gate.

12 ~~11~~. A detector according to Claim ~~10~~ 11, wherein a first one of said pair of AND gates is connected to two of said four bistable elements for receiving as inputs the two of the four local timing signals forming the pair of reference signals, and a second one of said pair of AND gates is connected to a remaining two of said four bistable elements for receiving as inputs logic complements of the remaining two timing signals.

13 ~~12~~. A detector for detecting timing in a data flow comprising:

a first circuit for generating four local timing signals each having a period substantially equal to a bit-time of the data flow, the four local timing signals being out of phase with one another by 1/4 period; and

a second circuit for determining based upon a sampling of the four local timing signals whether two of the four local timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow, and for controlling said first circuit to delay or advance the four local timing signals based upon the pair of reference signals.

14. A detector according to Claim 13, wherein the data flow comprises coding for providing at a beginning of the bit-time no transition, or the transition of a first type, or a transition of a second type, and providing in a middle of the bit-time no transition, or the transition of the first type.

15. A detector according to Claim 13, wherein the coding comprises a coded mark inversion coding.

16. A detector according to Claim 13, wherein said second circuit comprises:

a sampling circuit for sampling the four local timing signals upon each transition of the first type in the data flow; and

a decoding circuit connected to said sampling circuit for decoding the sampled four local timing signals.

17 ~~16~~. A detector according to Claim 16 ~~15~~, wherein said sampling circuit comprises four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow; and wherein said decoding circuit comprises a logic circuit connected to respective outputs of said four bistable elements for determining whether the pair of reference signals are advanced or delayed relative to the timing of the data flow.

18 ~~17~~. A detector according to Claim 17 ~~16~~, wherein each one of said bistable elements comprises a D-type flip-flop; and wherein said logic circuit comprises a pair of AND gates connected to the outputs of said four bistable elements, a NOR gate connected to respective outputs of said pair of AND gates, and an INVERTER connected to an output of said NOR gate.

19 ~~18~~. A detector according to Claim 17 ~~16~~, wherein a first one of said pair of AND gates is connected to two of said four bistable elements for receiving as inputs the two of the four local timing signals forming the pair of reference signals, and a second one of said pair of AND gates is connected to a remaining two of said four bistable elements for receiving as inputs logic complements of the remaining two timing signals.

20 ~~19~~. A data transmission network comprising:
a processing circuit for processing data;
a transmission medium; and

an interface circuit connected between said processing circuit and said transmission medium for interfacing a data flow therebetween, said interface circuit comprising a detector for detecting timing in the data flow, said detector comprising

a first circuit for generating four local timing signals each having a period substantially equal to a bit-time of the data flow, the four local timing signals being out of phase with one another by 1/4 period, and

a second circuit for determining based upon a sampling of the four local timing signals whether two of the four local timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow, and for controlling said first circuit to delay or advance the four local timing signals based upon the pair of reference signals.

21 ~~20~~. A data transmission network according to Claim 20 ~~19~~, wherein the data flow comprises coding for providing at a beginning of the bit-time no transition, or the transition of a first type, or a transition of a second type, and providing in a middle of the bit-time no transition, or the transition of the first type.

22 ~~21~~. A data transmission network according to Claim 21 ~~20~~, wherein the coding comprises a coded mark inversion coding.

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~~22~~. A data transmission network according to Claim 20 ~~19~~, further comprising a remote interface circuit connected to said transmission medium for receiving the data flow from said interface unit and for transmitting the data flow to said interface circuit.

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~~23~~. A data transmission network according to Claim 20 ~~19~~, wherein said processing circuit and said interface circuit conform to a synchronous digital hierarchy standard.

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~~24~~. A data transmission network according to Claim 20 ~~19~~, wherein said second circuit comprises:

a sampling circuit for sampling the four local timing signals upon each transition of the first type in the data flow; and

a decoding circuit connected to said sampling circuit for decoding the sampled four local timing signals.

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~~25~~. A data transmission network according to Claim 25 24, wherein said sampling circuit comprises four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow; and wherein said decoding circuit comprises a logic circuit connected to respective outputs of said four bistable elements for determining whether the pair of reference signals are advanced or delayed relative to the timing of the data flow.

27
~~26~~. A data transmission network according to Claim 26 25, wherein each one of said bistable elements comprises a D-

type flip-flop; and wherein said logic circuit comprises a pair of AND gates connected to the outputs of said four bistable elements, a NOR gate connected to respective outputs of said pair of AND gates, and an INVERTER connected to an output of said NOR gate.

27. A data transmission network according to Claim 26, wherein a first one of said pair of AND gates is connected to two of said four bistable elements for receiving as inputs the two of the four local timing signals forming the pair of reference signals, and a second one of said pair of AND gates is connected to a remaining two of said four bistable elements for receiving as inputs logic complements of the remaining two timing signals.

28. A method for detecting timing in a data flow comprising:

generating four local timing signals each having a period substantially equal to a bit-time of the data flow, the four local timing signals being out of phase with one another by 1/4 period;

sampling the four local timing signals upon each transition of a first type in the data flow;

determining based upon the sampling whether two of the four local timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow; and

delaying or advancing the four local timing signals based upon the pair of reference signals.

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~~29~~. A detector according to Claim ~~28~~, wherein the data flow comprises coding for providing at a beginning of the bit-time no transition, or the transition of the first type, or a transition of a second type, and providing in a middle of the bit-time no transition, or the transition of the first type.

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~~30~~. A detector according to Claim ~~28~~, wherein the coding comprises a coded mark inversion coding.

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~~31~~. A detector according to Claim ~~28~~, wherein after the sampling of the four local timing signals the method further comprises decoding the sampled four local timing signals.

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~~32~~. A detector according to Claim ~~31~~, wherein the sampling is performed by a sampling circuit comprising four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow; and wherein the decoding is performed using a logic circuit connected to respective outputs of the four bistable elements for determining whether the pair of reference signals are advanced or delayed relative to the timing of the data flow.

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~~33~~. A detector according to Claim ~~32~~, wherein a first one of said pair of AND gates is connected to two of the four bistable elements for receiving as inputs the two of the four local timing signals forming the pair of reference signals, and a second one of said pair of AND gates is connected to a remaining two of said four bistable elements